WHAT IS CLAIMED IS:

1. A semiconductor device having a static memory cell including:

a pair of driver transistors having gates and drains cross-coupled with each other;

a pair of access transistors having sources connected to said drains of said driver transistors respectively; and

a pair of load transistors having drains and gates connected to said drains of said driver transistors and said gates of said driver transistors respectively,

said semiconductor device comprising:

a first gate electrode part and a second gate electrode part formed at a space from each other across an element forming region formed on the main surface of a semiconductor substrate;

a first impurity region of a prescribed conductivity type formed on a portion of said element forming region held between said first gate electrode part and said second gate electrode part;

a second impurity region of said prescribed conductivity type formed on another potion of said element forming region located opposite to the side provided with said second gate electrode part with respect to said first gate electrode part;

an interlayer dielectric film formed on said semiconductor substrate to cover said first gate electrode part and said second gate electrode part;

a first opening formed in said interlayer dielectric film to continuously expose the upper surface of said second gate electrode part and the surface of said first impurity region;

a first gate side wall insulator film formed on the side surface of said second gate electrode part;

a first opening side wall insulator film formed on the side surface of said first opening;

a second gate side wall insulator film formed on the surface of said first side wall insulator film to cover the surface of a portion of a region of said semiconductor substrate located under said first gate side wall insulator film; and

a first conductor part formed to fill up said first opening for electrically connecting said first impurity region and said second gate electrode part with each other, wherein

the first one of said pair of load transistors includes said first gate electrode part, said first impurity region and said second impurity region, and

said second gate electrode part forming the gate of the second one of said pair of load transistors and said first impurity region of said first load transistor are electrically connected with each other through said first conductor part.

2. The semiconductor device according to claim 1, wherein

said first gate side wall insulator film, said first opening side wall insulator film and said second gate side wall insulator film are different in etching property from said interlayer dielectric film.

3. The semiconductor device according to claim 2, wherein

said first gate side wall insulator film, said first opening side wall insulator film and said second gate side wall insulator film include silicon nitride films, and said interlayer dielectric film includes a silicon oxide film.

4. The semiconductor device according to claim 1, further comprising:

a second opening formed in said interlayer dielectric film to expose the surface of said second impurity region,

a second opening side wall insulator film formed on the side surface of said second opening, and

a second conductor part formed to fill up said second opening.

5. The semiconductor device according to claim 1, further comprising metal silicide layers formed on the surface of said first impurity region, the surface of said second impurity region, the upper surface of said first gate electrode part and the upper surface of said second gate electrode part respectively.